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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HILTUNEN, THOMAS J	

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2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,450	HUANG ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/079,866.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's appeal brief filed October 15 2007 has been received. Examiner has found Applicant's arguments persuasive, thus prosecution has been reopened and new rejections of the claims submitted 14 February 2007 are provided below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-9, 11-17, 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Koizumi (USPN 5,296,757).

With respect to claims 1, 9 and 17, Koizumi discloses in Fig. 4, a phase-interpolation circuit (circuit of Fig. 4) for outputting a third clock signal (D) according to a first clock signal (A) and a second clock signal (B), the circuit comprising:

a first inverter for receiving the first clock signal (22 with 23 which receives signal C at its gate. However, signal C is essentially a buffered version of A, i.e., essentially the same as A. Furthermore, 22 and 23 receives A through 32 and 33);

a second inverter for receiving the second clock signal (12 with 13 which receive B);

wherein an output end of the second inverter is coupled to an output end of the first inverter to form a common output end to output the third clock signal (the drains of 12, 13, 22 and 23 are coupled together at a common node to output D);

a first controlled switch coupled to the first inverter, the second inverter, and a power source (11 with 12 coupled to the power source consisting of both VDD1 and VDD2), wherein the first controlled switch is "off' when the first clock signal is in a fist first state (A is high), and is "on" when the first clock signal is in a second state (A is low); and

a second controlled switch coupled to the first inverter, the second inverter, and ground (14 with 24 coupled to the ground supply of GND1 and GND), wherein the second controlled switch is "on" when the first clock signal is in the first state (A is high), and is "off' when the first clock signal is in the second state (A is low);

wherein the phase of the third clock signal is determined by the phase of the first clock signal and the second clock signal (the phase of D is determined by A and B); and

wherein the first controlled switch and the second controlled switch are serve to avoid a short-circuit current of the phase-interpolation circuit (the first and second switch serve to avoid a short in the circuit of Fig. 4).

With respect to claim 3, 11 and 19, Saeki discloses, the phase-interpolation circuit of claim 1, wherein the circuit further comprises:

a fourth inverter to output the first clock signal to the first inverter (one of 32 or 33); and a fifth inverter to output the second clock signal to the second inverter (31).

With respect to claim 4, 12 and 20, Saeki discloses, the phase-interpolation circuit of claim 1, wherein the first controlled switch comprises:

a first PMOS coupled between the first inverter and the power source, the first PMOS being "off" when the first clock signal is in the first state, and being "on" when the first clock signal is in the second state (11); and

a second PMOS coupled between the second inverter and the power source, the second PMOS being "off" when the first clock signal is in the first state, and being "on" when the first clock signal is in the second state (21).

With respect to claim 5, 13 and 21, Saeki discloses, the phase-interpolation circuit of claim 1, wherein the second controlled switch comprises:

a first NMOS coupled between the first inverter and the ground, the first NMOS being "off" when the first clock signal is in the second state, and being "on" when the first clock signal is in the first state (14); and

a second NMOS coupled between the second inverter and the ground, the second NMOS being "off' when the first clock signal is in the second state, and being "on" when the first clock signal is in the first state (24).

With respect to claims 6 and 14, the phase-interpolation circuit of claim 1, .wherein the first controlled switch at least includes a PMOS (one of 11 and 21).

With respect to claims 7 and 15, the phase-interpolation circuit of claim 1, wherein the second controlled switch at least includes a NMOS (one of 14 and 24).

With respect to claims 8, and 16, the phase-interpolation circuit of claim 1, wherein the first and the second inverter are CMOS inverters (the inverters are CMOS inverters).

Claims 1, 2, 4-10, 12-18 and 20-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Saeki (USPAPN 2002/0030525).

With respect to claims 1, 9 and 17, Saeki discloses in Fig. 6, a phase-interpolation circuit (circuit of Fig. 6) for outputting a third clock signal (OUT) according to a first clock signal (IN1) and a second clock signal (IN2), the circuit comprising:

a first inverter for receiving the first clock signal (MP52 with MN51);

a second inverter for receiving the second clock signal (MP54 with MN53);

wherein an output end of the second inverter is coupled to an output end of the first inverter to form a common output end to output the third clock signal (output node N52, which outputs the third clock OUT through INV51);

a first controlled switch coupled to the first inverter, the second inverter, and a power source (MP51 with MP53 coupled to Vcc), wherein the first controlled switch is "off' when the first clock signal is in a fist first state (high), and is "on" when the first clock signal is in a second state (low); and

a second controlled switch coupled to the first inverter, the second inverter, and ground (MN52 with MN54 coupled to ground), wherein the second controlled switch is

"on" when the first clock signal is in the first state (high), and is "off" when the first clock signal is in the second state (low);

wherein the phase of the third clock signal is determined by the phase of the first clock signal and the second clock signal (the phase of OUT is determined by IN1 and IN2); and

wherein the first controlled switch and the second controlled switch are serve to avoid a short-circuit current of the phase-interpolation circuit (the first and second switch serve to avoid a short in the circuit of Fig. 6).

With respect to claims 2, 10 and 18, Saeki discloses, the phase-interpolation circuit of claim 1, wherein the circuit further comprises a third inverter (INV51) coupled to the common output end (N52) to output the third clock signal (OUT).

With respect to claim 4, 12 and 20, Saeki discloses, the phase-interpolation circuit of claim 1, wherein the first controlled switch comprises:

a first PMOS coupled between the first inverter and the power source, the first PMOS being "off" when the first clock signal is in the first state, and being "on" when the first clock signal is in the second state (MP51); and

a second PMOS coupled between the second inverter and the power source, the second PMOS being "off" when the first clock signal is in the first state, and being "on" when the first clock signal is in the second state (MP53).

With respect to claim 5, 13 and 21, Saeki discloses, the phase-interpolation circuit of claim 1, wherein the second controlled switch comprises:

a first NMOS coupled between the first inverter and the ground, the first NMOS being "off" when the first clock signal is in the second state, and being "on" when the first clock signal is in the first state (MN52); and

a second NMOS coupled between the second inverter and the ground, the second NMOS being "off' when the first clock signal is in the second state, and being "on" when the first clock signal is in the first state (MN54).

With respect to claims 6 and 14, the phase-interpolation circuit of claim 1, .wherein the first controlled switch at least includes a PMOS (one of MP51 and MP53).

With respect to claims 7 and 15, the phase-interpolation circuit of claim 1, wherein the second controlled switch at least includes a NMOS (one of MN52 and MN54).

With respect to claims 8, and 16, the phase-interpolation circuit of claim 1, wherein the first and the second inverter are CMOS inverters (the inverters are CMOS inverters).

Claims 1, 2, 4-10, 12-18 and 20-21 are rejected under 35 U.S.C. 102(a) as being anticipated by Saeki (JP2002-14743).

With respect to claims 1, 9 and 17, Saeki discloses in Fig. 6, a phase-interpolation circuit (circuit of Fig. 6) for outputting a third clock signal (OUT) according to a first clock signal (IN1) and a second clock signal (IN2), the circuit comprising:

a first inverter for receiving the first clock signal (MP52 with MN51);

a second inverter for receiving the second clock signal (MP54 with MN53);

wherein an output end of the second inverter is coupled to an output end of the first inverter to form a common output end to output the third clock signal (output node N52, which outputs the third clock OUT through INV51);

a first controlled switch coupled to the first inverter, the second inverter, and a power source (MP51 with MP53 coupled to Vcc), wherein the first controlled switch is "off' when the first clock signal is in a fist first state (high), and is "on" when the first clock signal is in a second state (low); and

a second controlled switch coupled to the first inverter, the second inverter, and ground (MN52 with MN54 coupled to ground), wherein the second controlled switch is "on" when the first clock signal is in the first state (high), and is "off' when the first clock signal is in the second state (low);

wherein the phase of the third clock signal is determined by the phase of the first clock signal and the second clock signal (the phase of OUT is determined by IN1 and IN2); and

wherein the first controlled switch and the second controlled switch are serve to avoid a short-circuit current of the phase-interpolation circuit (the first and second switch serve to avoid a short in the circuit of Fig. 6).

With respect to claims 2, 10 and 18, Saeki discloses, the phase-interpolation circuit of claim 1, wherein the circuit further comprises a third inverter (INV51) coupled to the common output end (N52) to output the third clock signal (OUT).

With respect to claim 4, 12 and 20, Saeki discloses, the phase-interpolation circuit of claim 1, wherein the first controlled switch comprises:

a first PMOS coupled between the first inverter and the power source, the first PMOS being "off" when the first clock signal is in the first state, and being "on" when the first clock signal is in the second state (MP51); and

a second PMOS coupled between the second inverter and the power source, the second PMOS being "off" when the first clock signal is in the first state, and being "on" when the first clock signal is in the second state (MP53).

With respect to claim 5, 13 and 21, Saeki discloses, the phase-interpolation circuit of claim 1, wherein the second controlled switch comprises:

a first NMOS coupled between the first inverter and the ground, the first NMOS being "off" when the first clock signal is in the second state, and being "on" when the first clock signal is in the first state (MN52); and

a second NMOS coupled between the second inverter and the ground, the second NMOS being "off' when the first clock signal is in the second state, and being "on" when the first clock signal is in the first state (MN54).

With respect to claims 6 and 14, the phase-interpolation circuit of claim 1, .wherein the first controlled switch at least includes a PMOS (one of MP51 and MP53).

With respect to claims 7 and 15, the phase-interpolation circuit of claim 1, wherein the second controlled switch at least includes a NMOS (one of MN52 and MN54).

With respect to claims 8, and 16, the phase-interpolation circuit of claim 1, wherein the first and the second inverter are CMOS inverters (the inverters are CMOS inverters).

It is noted that Applicant has not filed an English translation of the foreign priority documents of Taiwanese application number 90104097 in the both the instant application and U.S. patent application No. 10/079,866. Therefore, the claimed foreign priority date of 22 February 2001 of the instant application cannot be granted. Furthermore, it is noted that Saeki (USPAPN 2002/0030525) claims foreign priority to 27 April 2000.

Claim Rejections - 35 USC § 103

Claims 3, 11 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saeki (USPAPN 2002/0030525).

Claims 2, 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi (USPN 5,296,757).

With respect to claims 2, 10 and 18, Koizumi fails to disclose, the phase-interpolation circuit of claim 1, wherein the circuit further comprises a third inverter coupled to the common output end to output the third clock signal.

However, it is old and well known to buffer output signals with an inverter, which has a high input impedance and low output impedance, to prevent loading between circuits and to avoid mismatched impedance between a circuit's output signal and the circuit receiving the output signal. It would have been obvious to one of ordinary skill in the art at the time of the invention to add at least one inverter to buffer the output signal D of Fig. 4 of Koizumi to prevent loading between the output signal D of Koizumi and the circuit receiving D.

With respect to claim 3, 11 and 19, Saeki fails to disclose, the phase-interpolation circuit of claim 1, wherein the circuit further comprises:

a fourth inverter to output the first clock signal to the first inverter; and a fifth inverter to output the second clock signal to the second inverter.

However, it is old and well known to buffer input signals with inverters, which have a high input impedance and low output impedance, to prevent loading between circuits and to avoid mismatched impedance between a circuit outputting clock signals and a circuit receiving the clock signals. It would have been obvious to one of ordinary skill in the art at the time of the invention to supply the input clocks of IN1 and IN2 via inverters to the circuit of Fig. 6 of Saeki to decrease signal degradation and avoid loading between the circuits supplying the clock signals and the circuit of Fig. 6 of Saeki.

Response to Arguments

Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Cited Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kuhn, Jr. et al. (USPN 3,890,580) discloses in Col. 3 lines 36-39 that it is old and well known that inverters have high input impedance and low output impedance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on M-F 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TH
December 21, 2007

N. DREW RICHARDS
SUPERVISORY PATENT EXAMINER